

TRANSISTOR ARRAY AND METHOD OF LAYOUT

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to transistor arrays, and more particularly, to transistor arrays arranged in consideration of error value on a single chip.

Description of Related Art

 A layout method for a conventional transistor array is explained below with
10 reference to an exemplary transistor array of a flash type digital to analog ("D/A") converting circuit that receives an 8-bit digital signal and converts it to generate an analog signal having 256 various levels.

 FIG. 1 shows a configuration of a conventional digital to analog converting circuit. The D/A converting circuit of FIG. 1 includes four-to-fifteen type converters 10-1 and 10-
15 2, an MSB transistor array 20-1, an LSB transistor array 20-2, MSB switches 30-1, and LSB switches 30-2.

 As shown in FIG. 1, the MSB transistor array 20-1 includes transistors M1 to M15, and the LSB transistor array 20-2 includes transistors L1 to L15. The size of each of the transistors M1 to M15 of the MSB transistor array 20-1 is 16 times as large as
20 that of each of the transistors L1 to L15 of the LSB transistor array 20-2. That is, 16 LSB-sized transistors constitute a single MSB transistor. Each of the transistors M1 to M15 and L1 to L15 includes an NMOS transistor having a drain to which a power voltage VCC is applied, and a gate to which a bias voltage is applied. The MSB

switches 30-1 include switches MS1 to MS15 connected between the respective transistors M1 to M15 and a terminal for generating an output signal Aout, and the LSB switches 30-2 include switches LS1 to LS15 connected between the respective transistors L1 to L15 and the terminal for generating the output signal Aout.

5 Operation of the components of the D/A converting circuit of FIG. 1 is explained below.

 The four-to-fifteen type converter 10-1 converts an upper 4-bits B8 to B5 of an 8-bit digital signal B8 to B1 to generate a 15-bit digital signal MO1 to MO15. When the upper 4-bits B8 to B5 are "0000", the digital signal MO1 to MO15 of "00...0" is
10 generated. And, when the upper 4-bits B8 to B5 are "0001", the digital signal MO1 to MO15 of "00...1" is generated. Also, when the digital signal B8 to B5 is "0011", the digital signal MO1 to MO15 of "00...011" is generated. That is, whenever the digital signal B8 to B5 is increased by 1, a bit number of "1" of the digital signal MO1 to MO15 is increased by 1. The four-to-fifteen type converter 10-2 converts a lower 4-bits B4 to
15 B1 of an 8-bit digital signal B8 to B1 to generate a 15-bit digital signal LO1 to LO15. The transistors M1 to M15 allow a constant amount of electric current to flow, and the transistors L1 to L15 also allow a constant amount of electric current to flow. Here, since a size of each of the transistors M1 to M15 is 16 times as large as that of each of the transistors L1 to L15, an amount of electric current flowing along each of the transistors
20 M1 to M15 is 16 times as much as that flowing along each of the transistors L1 to L15. The MSB switches MS1 to MS15 are each turned on when each of the digital signals MO1 to MO15, respectively, have a high level, allowing an electric current to flow to the terminal for generating the output signal Aout. The LSB switches LS1 to LS15 are each

turned on when each of the digital signals LO1 to LO15, respectively, have a high level, allowing an electric current to flow to the terminal for generating the output signal Aout. An electric current through the MSB switches 30-1 and an electric current through the LSB switches 30-2 join and flow to the terminal for generating the output signal Aout. A current outputted through the terminal for generating the output signal Aout has a total of 256 levels. At this time, a difference between current levels should be uniform.

However, in the conventional layout method of the MSB and LSB transistor array, analog signals outputted from the output signal (Aout) generating terminal do not have a uniform level difference.

FIG. 2 shows an example of a layout method of the MSB and LSB transistor array of the flash type D/A converting circuit of FIG. 1. In FIG. 2, the transistor array has 16 rows and 16 columns.

In FIG. 2, T1,1 to Tn,n denote an array area. A digit next to "T" denotes a row, and a next digit denotes a column. For example, T1,1 denotes an array area located at a first row and a first column.

A layout method of the transistor array of FIG. 2 is explained below.

The MSB transistor M1 is arranged on each of the areas T1,1, T2,1, ..., T16,1, which are each the same size as an LSB transistor. The MSB transistor M2 is arranged on each of the areas T2,2, ..., T16,2 and T1,2, which are each the same size as an LSB transistor. The MSB transistor M15 is arranged on each of the areas T2,15, ..., T16,15 and T1,15, which are each the same size as an LSB transistor. 16 transistors which constitute each of the MSB transistors M1 to M15 are arranged in the same column, forming a line. The LSB transistors L1 to L15 are, respectively, arranged on the areas

T2,16, ..., T15,16, and T1,16. Thus, the LSB transistors L1 to L15 are arranged in a 16th column, forming a line.

The layout method of FIG. 2 has a problem in that transistors of the transistor array do not have the same operational characteristics since the transistors of the transistor array have different temperature distributions and process variations according to their arranged location. That is, the transistors of the transistor array have an error value that varies with a temperature distribution and a process variation. Therefore, signals outputted from the transistor array could not be generated to have a uniform level difference.

FIG. 3 shows another layout method of the MSB and LSB transistor array of the flash type D/A converting circuit of FIG. 1. As shown in FIG. 3, a single transistor is arranged on each of the array areas T1,1 to T16,15.

The layout method of FIG. 3 is explained below.

The LSB transistors L1 to L15 are arranged on the areas T1,8, T2,8, ..., T15,8 and T16,8, respectively. That is, the LSB transistors L1 to L15 are arranged in the 8th column, forming a line. The MSB transistor M1 is arranged on each of the areas T1,1, ... T7,7, T9,9, ... ,T15,15, and T16,1, which are each the same size as an LSB transistor. The MSB transistor M2 is arranged on each of the areas T1,15, T2,1, ..., T8,7, T10,9 ..., T16,15, which are each the same size as an LSB transistor. The MSB transistor M15 is arranged on each of the areas T1,2, ..., T6,7, T8,9 ...T14,15, T15,1, and T16,2, which are each the same size as an LSB transistor. In the same way, the rest of the MSB transistors M3 to M14 are also arranged in a diagonal direction. That

is, the MSB transistors M1 to M15 are arranged in the areas along diagonal directions while skipping the 8th column.

The layout methods of FIGs. 2 and 3 are described in United States Patent No. 5,568,145.

5 To solve a problem of the layout method of FIG. 2, the layout method of FIG. 3 arranges each of the MSB transistors M1 to M15, which are turned on simultaneously, in a diagonal direction to reduce the effects of temperature distribution and process variation.

10 However, since the LSB transistors L1 to L15 are arranged only in a central portion, such arrangement cannot remove the effects of temperature distribution and process variation. Therefore, signals outputted from the transistor array can not be generated with a uniform level difference.

SUMMARY OF THE INVENTION

15 It is a feature of the present invention to provide a transistor array in which transistors are arranged to minimize the effects of temperature distribution and process variation, thereby generating signals having a uniform level difference therefrom.

20 It is another feature of the present invention to provide a layout method of a transistor array in which transistors are arranged to minimize the effects of temperature distribution and process variation, thereby generating signals having a uniform level difference therefrom.

In order to realize the above features, preferred embodiments of the present invention provide a transistor array, comprising a plurality of LSB transistors arranged

along diagonal directions of a central portion of an array including a plurality of rows and a plurality of columns; and a plurality of MSB transistors arranged, respectively, along diagonal directions above and below the plurality of LSB transistors.

The present invention further provides a transistor array, comprising a plurality of

5 first LSB transistors arranged along diagonal directions of a central portion of a first quadrant of an array including a plurality of rows and a plurality of columns; a plurality of first MSB transistors arranged along diagonal directions respectively above and below the plurality of first LSB transistors; a plurality of second LSB transistors and a plurality of second MSB transistors arranged on a second quadrant of the array to be

10 symmetrical in a Y-axis direction to the plurality of first LSB transistor and the plurality of first MSB transistors; a plurality of third LSB transistors and a plurality of third MSB transistors arranged on a third quadrant of the array to be symmetrical in an X-axis direction to the plurality of first LSB transistor and the plurality of first MSB transistors; and a plurality of fourth LSB transistors and a plurality of fourth MSB transistors

15 arranged on a fourth quadrant of the array to be symmetrical in a Y-axis direction to the plurality of third LSB transistors and the plurality of third MSB transistors.

The present invention further provides a layout method of a transistor array, comprising arranging a plurality of LSB transistors along diagonal directions of a central portion of an array including a plurality of rows and a plurality of columns; and arranging

20 a plurality of MSB transistors, respectively, along diagonal directions above and below the plurality of LSB transistors.

The present invention further provides a layout method of a transistor array, comprising arranging a plurality of first LSB transistors along diagonal directions of a

central portion of a first quadrant of an array including a plurality of rows and a plurality of columns; arranging a plurality of first MSB transistors along diagonal directions, respectively, above and below the plurality of first LSB transistors; arranging a plurality of second LSB transistors and a plurality of second MSB transistors on a second quadrant of the array to be symmetrical in a Y-axis direction to the plurality of first LSB transistors and the plurality of first MSB transistors; arranging a plurality of third LSB transistors and a plurality of third MSB transistors on a third quadrant of the array to be symmetrical in an X-axis direction to the plurality of first LSB transistors and the plurality of first MSB transistors; and arranging a plurality of fourth LSB transistors and a plurality of fourth MSB transistors on a fourth quadrant of the array to be symmetrical in a Y-axis direction to the plurality of third LSB transistors and the plurality of third MSB transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

FIG. 1 is a configuration of a conventional digital to analog converting circuit;

FIG. 2 shows an example of a conventional layout method of a MSB and LSB transistor array of the flash type D/A converting circuit of FIG. 1;

FIG. 3 shows another conventional layout method of a MSB and LSB transistor array of the flash type D/A converting circuit of FIG. 1;

FIGs. 4a and 4b are graphs showing systematic and graded error distributions according to locations of transistors arranged in a single chip, respectively;

FIG. 5 is a graph showing an error distribution obtained by linearizing and modeling the systematic error distribution of FIG. 4a;

5 FIG. 6 shows error values according to an arrangement location of the transistors by the error values shown in the graph of FIG. 5;

FIG. 7 shows a layout method of a transistor array according to the present invention; and

10 FIG. 8 shows another layout method of the transistor array according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

15 The present invention teaches a layout method of a transistor array using systematic and graded error distributions, which show an error distribution according to a temperature distribution and process variation.

20 FIGs. 4a and 4b are graphs showing systematic and graded error distributions according to locations of transistors arranged in a single chip, respectively. In FIGs. 4a and 4b, an underside denotes a location of transistors arranged in a single chip, and a vertical axis denotes error values for respective locations of transistors.

As shown in FIG. 4a, transistors arranged on a central portion have error values from 0.1 to 1.0, and have larger error values for transistors more distant from a central

portion. The transistors arranged on an edge portion have an error value of 0.9 to 1.0. That is, the error distribution of FIG. 4a shows a spatial distribution.

As shown in FIG. 4b, transistors arranged on a central portion have an error value of 0.0. The transistors have larger error values for transistors more distant from a central portion to a right side, and the transistors have smaller error values for transistors more distant from a central portion to a left side. That is, the error distribution of FIG. 4b shows a plane distribution.

FIG. 5 is a graph showing an error distribution obtained by linearizing and modeling the systematic error distribution of FIG. 4a. In FIG. 5, weighted error values range from -15 to 15 by applying a weighting factor to the error values.

As can be seen in FIG. 5, the error values of the transistors arranged on a central portion of the transistor array ranges from -15 to -10, and the error values become generally larger as the transistors become farther from the central portion. That is, the error values of the transistors arranged on an edge portion range from 10 to 15.

FIG. 6 shows error values according to an arrangement location of the transistors by the error values shown in the graph of FIG. 5.

As shown in FIG. 6, the chip with the transistor array arranged thereon is divided into 32×32 areas on which the error value is written. Areas of a diagonal direction of a first quadrant 40-1 inclined to a right side, areas of a diagonal direction of a second quadrant 40-2 inclined to a left side, areas of a diagonal direction of a third quadrant 40-3 inclined to a left, and areas of a diagonal direction of a fourth quadrant 40-4 inclined to a right side have an error value of "0". Areas of a nearest inside diagonal direction to the diagonal direction areas having an error value of "0" have an error value of "-1", and

areas of a farthest inside diagonal direction have an error value of “-15”. That is, the error value is decreased by “1” as it is inwardly displaced from the area having an error value of “0”. Areas of a nearest outside diagonal direction to the diagonal direction areas having an error value of “0” have an error value of “1”, and areas of a farthest outside diagonal direction have an error value of “15”. That is, the error value is increased by “1” as it is outwardly displaced from the area having an error value of “0”.

FIG. 7 shows a layout method of a transistor array according to the present invention. The LSB transistors L1 to L15 of FIG. 1 are arranged on areas of a diagonal direction, forming a line, and the MSB transistors M1 to M15 are arranged on upper and lower areas, respectively, centering on the diagonal line formed by the LSB transistors L1 to L15.

In more detail, the LSB transistors L1 to L15 are arranged on the areas T1,16, T2,15, ..., T16,1, forming a line. The MSB transistors M1 are arranged on each of the areas T1,15, ..., T15,1, and T16,16 which are each the same size as an LSB transistor. The MSB transistors M2 are arranged on each of the areas T1,14, T2,13, ..., T14,1, T15,16, and T16,15 which are each the same size as an LSB transistor. The transistors M15 are arranged on each of the areas T2,6, T3,15, ..., T16,2, and T1,1 which are each the same size as an LSB transistors. The other MSB transistors M3 to M14 are also arranged in a diagonal direction. That is, the MSB transistors M1 to M15 above the LSB transistors are arranged in increasing numerical order from the diagonal direction areas T1,15 to T15,1 close to the LSB transistors L1 to L15 to an edge area T1,1. The MSB transistors M1 to M15 below the LSB transistors are arranged reversely or in decreasing

numerical order from the diagonal direction areas T2,16 to T16,2 close to the LSB transistors L1 to L15 to an edge area T16,16.

That is, in the layout method of FIG. 7, the LSB transistors L1 to L15 respectively have an error value of "0", and a sum total of the error values of the transistors of each of the MSB transistors M1 to M15 is all "0".

The layout method of FIG. 7 can reduce the effects of temperature distribution and process variation because the LSB transistors L1 to L15 as well as the MSB transistors M1 to M15 are arranged in a diagonal direction.

However, the layout method of FIG. 7 may not perfectly remove all effects of temperature distribution and process variation because it does not have a completely symmetrical structure.

FIG. 8 shows another layout method of a transistor array according to the present invention. Each of the MSB transistors M1 to M15 of FIG. 7 includes 16 LSB-sized transistors, but each of the MSB transistors M1 to M15 of FIG. 8 includes 64 LSB-sized transistors. A size of a transistor arranged on a single grid area shown in FIG. 8 is a quarter of that of a transistor of FIG. 7.

The layout method of FIG. 8 arranges a transistor array in consideration of error values of FIG. 6 such that an error value of each of the LSB transistors L1 to L15 is "0", and a sum total of error values of 64 transistors which constitute each of the MSB transistors M1 to M15 is "0".

That is, the transistor array of a first quadrant 40-1 is arranged in the same way as the layout method of FIG. 7. The transistor array of a second quadrant 40-2 is arranged to be symmetric in a Y-axis direction to the transistor array of the first quadrant

40-1. The transistor array of a third quadrant 40-3 is arranged to be symmetric in an X-axis direction to the transistor array of the first quadrant 40-1. The transistor array of a fourth quadrant 40-4 is arranged to be symmetric in a Y-axis direction to the transistor array of the third quadrant 40-3.

5 The layout method of FIG. 8 can minimize the effects of temperature distribution and process variation by a completely symmetrical arrangement of the LSB and MSB transistors based on the error values according to locations of the transistors.

 Therefore, signals outputted from the transistor array can be generated with a uniform level difference.

10 As will be recognized by those of ordinary skill in the pertinent art, the present invention is described for exemplary transistor arrays, but can be similarly applied to the layout method of a capacitor array, for example.

 As described herein, the transistor array and the layout method of the transistor array according to the present invention can minimize the effects of temperature
15 distribution and process variation. Accordingly, a circuit element like a flash type D/A converting circuit having the transistor array of the present invention can have improved operation characteristics.

 While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those of ordinary skill in the
20 pertinent art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention, as set forth in the appended claims.